Lógica Digital (1001351)

Síntese lógica

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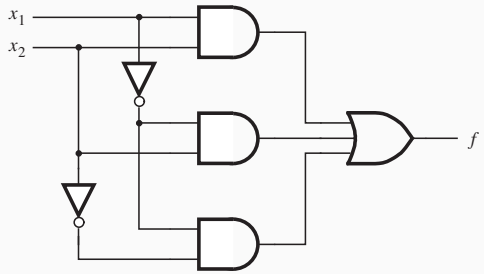
Síntese Lógica

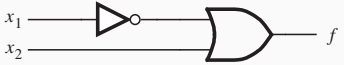
x_1	x_2	$f(x_1, x_2)$
0	0	1
0	1	1
1	0	0
1	1	1

$$f(x_1, x_2) = x_1x_2 + \overline{x}_1\overline{x}_2 + \overline{x}_1x_2$$
$$f(x_1, x_2) = x_1x_2 + \overline{x}_1\overline{x}_2 + \overline{x}_1x_2 + \overline{x}_1x_2$$
$$f(x_1, x_2) = x_1x_2 + \overline{x}_1x_2 + \overline{x}_1\overline{x}_2 + \overline{x}_1x_2$$
$$f(x_1, x_2) = (x_1 + \overline{x}_1)x_2 + \overline{x}_1(\overline{x}_2 + x_2)$$
$$f(x_1, x_2) = 1.x_2 + \overline{x}_1.1 \; f(x_1, x_2) = x_2 + \overline{x}_1$$

Figure 2.19 A function to be synthesized.



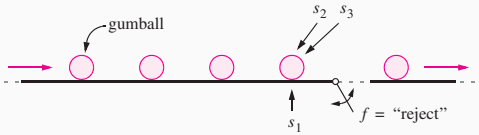
(a) Canonical sum-of-products



(b) Minimal-cost realization

Figure 2.20 Two implementations of the function in Figure 2.19.

Síntese Lógica



(a) Conveyor and sensors

s_1	s_2	s_3	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(b) Truth table

$f(s_1, s_2, s_3) = \bar{s}_1\bar{s}_2s_3 + \bar{s}_1s_2s_3 + s_1\bar{s}_2s_3 + s_1s_2\bar{s}_3 + s_1s_2s_3$

$\bar{s}_1\bar{s}_2s_3 + \bar{s}_1s_2s_3 + s_1\bar{s}_2s_3 + s_1s_2s_3 + s_1s_2\bar{s}_3 + s_1s_2s_3$
$\bar{s}_1s_3(\bar{s}_2 + s_2) + s_1s_3(\bar{s}_2 + s_2) + s_1s_2(\bar{s}_3 + s_3)$
$\bar{s}_1s_3 + s_1s_3 + s_1s_2$
$s_3 + s_1s_2$

ou

$\bar{s}_1\bar{s}_2s_3 + \bar{s}_1s_2s_3 + s_1\bar{s}_2s_3 + s_1s_2s_3 + s_1s_2\bar{s}_3 + s_1s_2s_3$
$s_3(\bar{s}_1\bar{s}_2 + \bar{s}_1s_2 + s_1\bar{s}_2 + s_1s_2) + s_1s_2(\bar{s}_3 + s_3)$
$s_3.1 + s_1s_2$
$s_3 + s_1s_2$

ou

$\bar{s}_1\bar{s}_2s_3 + \bar{s}_1s_2s_3 + s_1\bar{s}_2s_3 + \bar{s}_1\bar{s}_2s_3 + s_1s_2\bar{s}_3 + s_1s_2s_3$
$\bar{s}_1s_3(s_2 + \bar{s}_2) + \bar{s}_2s_3(s_1 + \bar{s}_1) + s_1s_2(s_3 + \bar{s}_3)$
$\bar{s}_1s_3 + \bar{s}_2s_3 + s_1s_2$
$s_3(\bar{s}_1 + \bar{s}_2) + s_1s_2$
$s_3(\overline{s_1s_2}) + s_1s_2$
$s_3 + s_1s_2$

Mintermos e maxtermos

Row number	x_1	x_2	x_3	Minterm	Maxterm
0	0	0	0	$m_0 = \bar{x}_1\bar{x}_2\bar{x}_3$	$M_0 = x_1 + x_2 + x_3$
1	0	0	1	$m_1 = \bar{x}_1\bar{x}_2x_3$	$M_1 = x_1 + x_2 + \bar{x}_3$
2	0	1	0	$m_2 = \bar{x}_1x_2\bar{x}_3$	$M_2 = x_1 + \bar{x}_2 + x_3$
3	0	1	1	$m_3 = \bar{x}_1x_2x_3$	$M_3 = x_1 + \bar{x}_2 + \bar{x}_3$
4	1	0	0	$m_4 = x_1\bar{x}_2\bar{x}_3$	$M_4 = \bar{x}_1 + x_2 + x_3$
5	1	0	1	$m_5 = x_1\bar{x}_2x_3$	$M_5 = \bar{x}_1 + x_2 + \bar{x}_3$
6	1	1	0	$m_6 = x_1x_2\bar{x}_3$	$M_6 = \bar{x}_1 + \bar{x}_2 + x_3$
7	1	1	1	$m_7 = x_1x_2x_3$	$M_7 = \bar{x}_1 + \bar{x}_2 + \bar{x}_3$

Figure 2.22 Three-variable minterms and maxterms.

Formas canônicas

Row number	x_1	x_2	x_3	$f(x_1, x_2, x_3)$
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

Figure 2.23 A three-variable function.

Soma dos produtos:

$$f(x_1, x_2, x_3) = \Sigma(m_1, m_4, m_5, m_6)$$

$$f(x_1, x_2, x_3) = \Sigma m(1, 4, 5, 6)$$

Produto das somas:

$$f(x_1, x_2, x_3) = \Pi(M_0, M_2, M_3, M_7)$$

$$f(x_1, x_2, x_3) = \Pi M(0, 2, 3, 7)$$

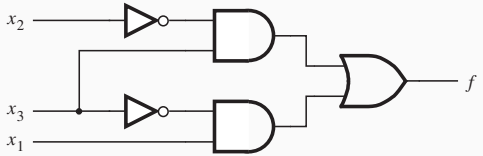
Formas canônicas

Row number	x_1	x_2	x_3	$f(x_1, x_2, x_3)$
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

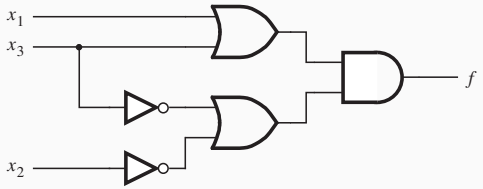
Figure 2.23 A three-variable function.

$$\overline{f} = m_0 + m_2 + m_3 + m_7$$
$$f = \overline{m_0 + m_2 + m_3 + m_7}$$
$$f = \overline{m}_0\overline{m}_2\overline{m}_3\overline{m}_7$$
$$f = M_0.M_2.M_3.M_7$$

Implementações possíveis para a função



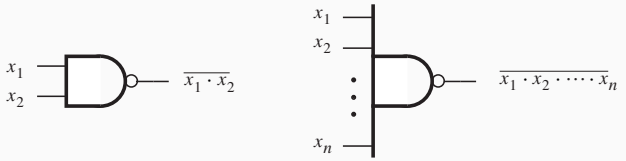
(a) A minimal sum-of-products realization



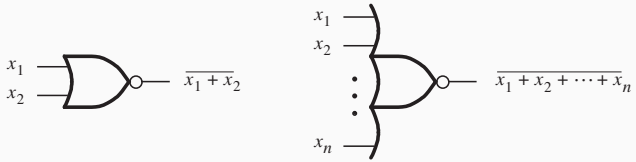
(b) A minimal product-of-sums realization

Figure 2.24 Two realizations of the function in Figure 2.23.

Portas NAND e NOR



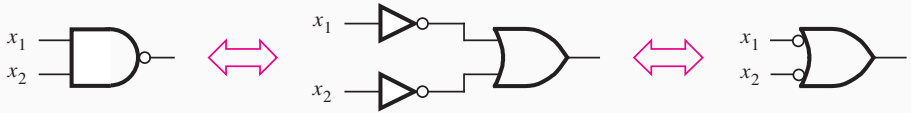
(a) NAND gates



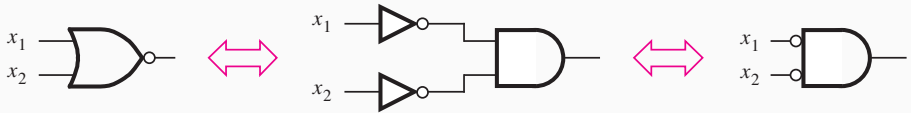
(b) NOR gates

Figure 2.25 NAND and NOR gates.

Teorema DeMorgan



(a) $\overline{x_1 x_2} = \bar{x}_1 + \bar{x}_2$



(b) $\overline{x_1 + x_2} = \bar{x}_1 \bar{x}_2$

Figure 2.26 DeMorgan's theorem in terms of logic gates.

Exemplos

Exemplos

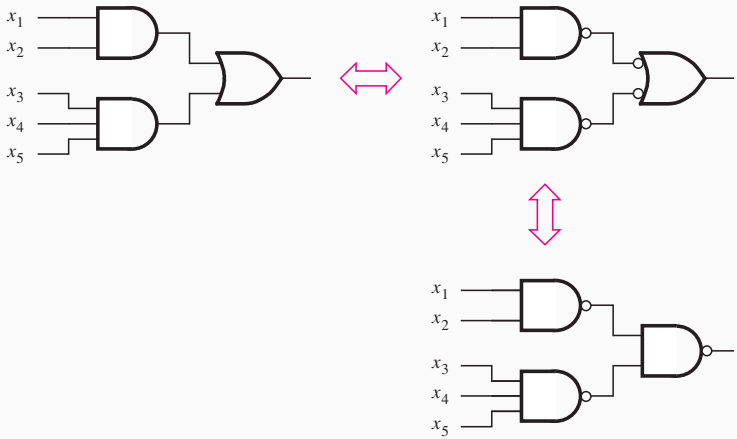


Figure 2.27 Using NAND gates to implement a sum-of-products.

Exemplos

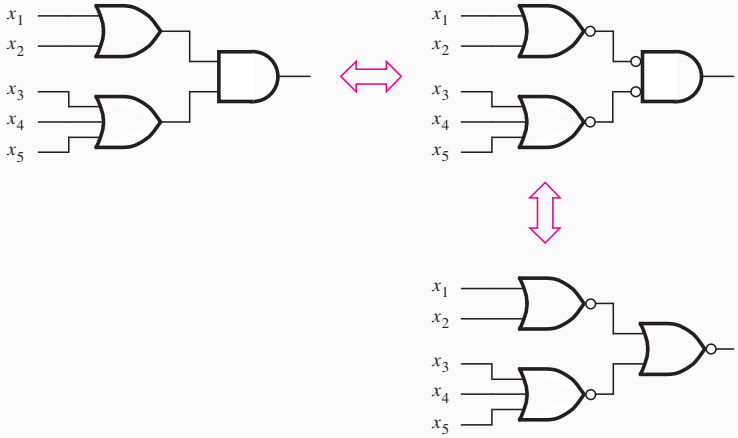
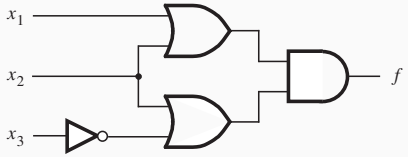
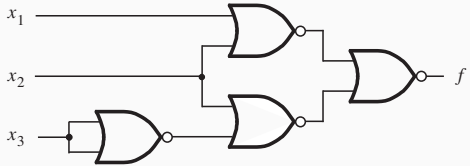


Figure 2.28 Using NOR gates to implement a product-of-sums.

Exemplos



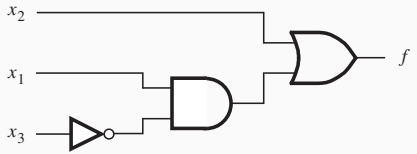
(a) POS implementation



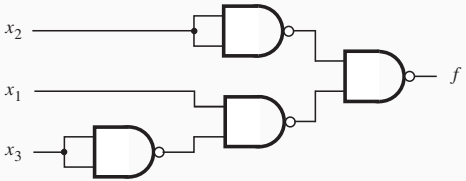
(b) NOR implementation

Figure 2.29 NOR-gate realization of the function in Example 2.13.

Exemplos



(a) SOP implementation



(b) NAND implementation

Figure 2.30 NAND-gate realization of the function in Example 2.10.

Bibliografia

Bibliografia

- Brown, S. & Vranesic, Z. - Fundamentals of Digital Logic with Verilog Design, 3rd Ed., Mc Graw Hill, 2009

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