Lógica Digital (1001351)

Circuitos Sequenciais: Latches e Flip-flops

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Circuitos Sequenciais

Objetivos

Nesta aula vamos aprender sobre:

- Circuitos lógicos que podem armazenar informações;
- Latches e Flip-flops, os quais armazenam um único bit.

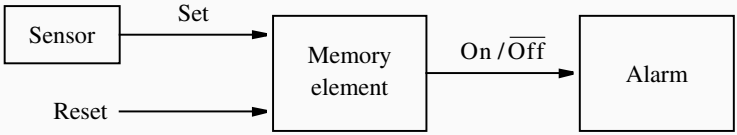


Figure 5.1 Control of an alarm system.

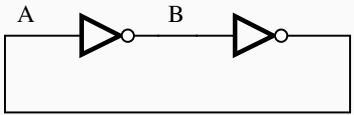
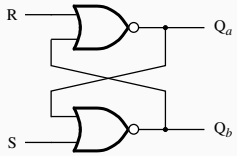


Figure 5.2 A simple memory element.

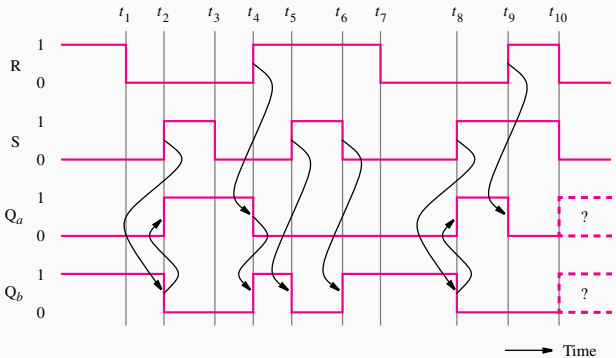
Latch básico



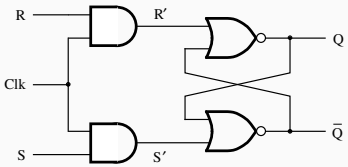
(a) Circuit

S	R	Q_a	Q_b	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

(b) Characteristic table



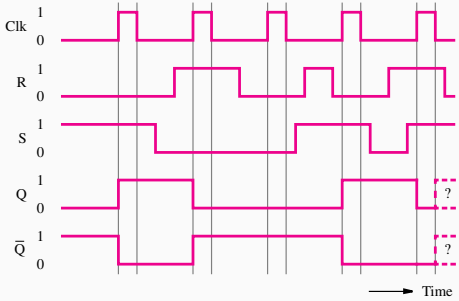
Latch com habilita *(gated latch)*



(a) Circuit

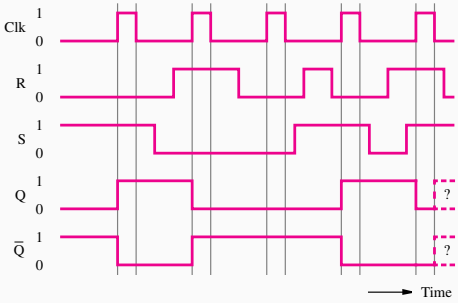
Clk	S	R	Q(*t* + 1)
0	x	x	Q(*t*) (no change)
1	0	0	Q(*t*) (no change)
1	0	1	0
1	1	0	1
1	1	1	x

(b) Characteristic table



(c) Timing diagram

Latch com habilita *(gated latch)*



(c) Timing diagram

(d) Graphical symbol

Figure 5.5 Gated SR latch.

Latch construído com portas NAND

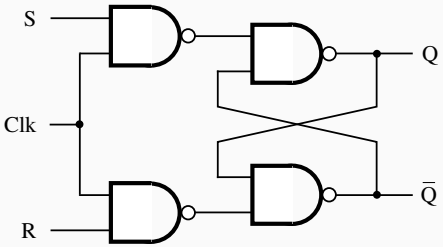
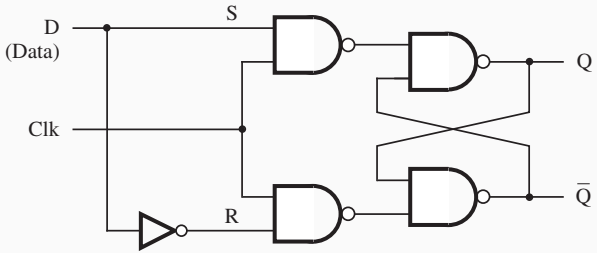


Figure 5.6 Gated SR latch with NAND gates.

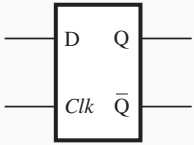
Latch D



(a) Circuit

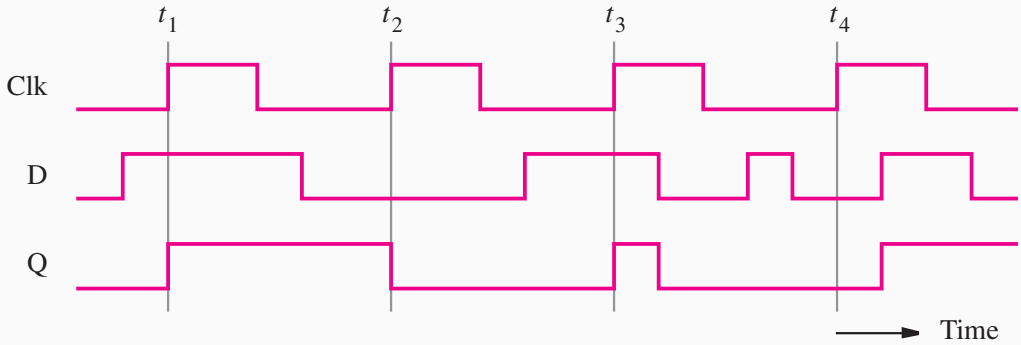
Clk	D	Q(t + 1)
0	x	Q(t)
1	0	0
1	1	1

(b) Characteristic table



(c) Graphical symbol

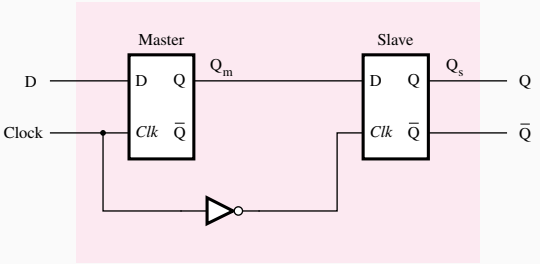
Latch D



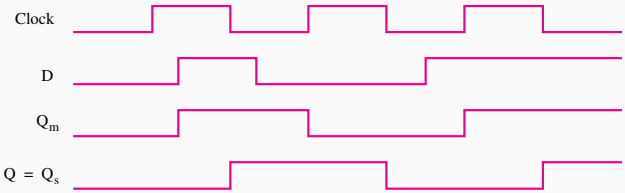
(d) Timing diagram

Figure 5.7 Gated D latch.

Flip-flop D Mestre/Escravo

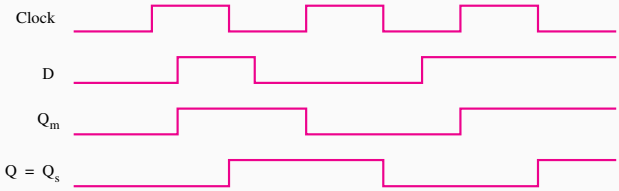


(a) Circuit

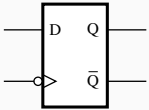


(b) Timing diagram

Flip-flop D Mestre/Escravo



(b) Timing diagram



(c) Graphical symbol

Figure 5.9 Master-slave D flip-flop.

Flip-flop D com borda positiva (subida)

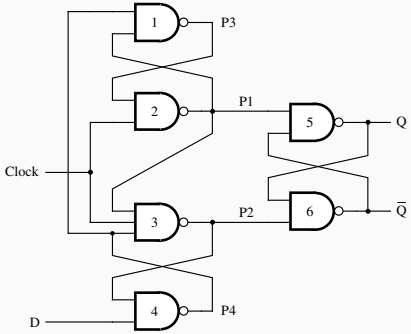
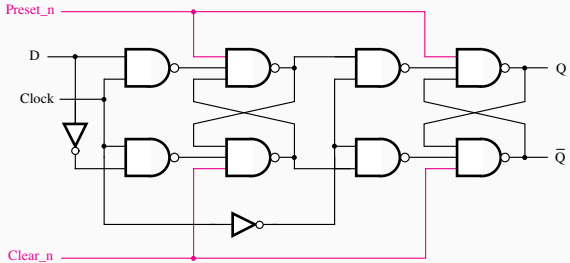
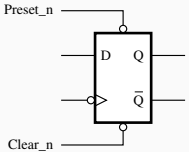


Figure 5.11 A positive-edge-triggered D flip-flop.

Flip-flop D Mestre/Escravo com Clear e Preset



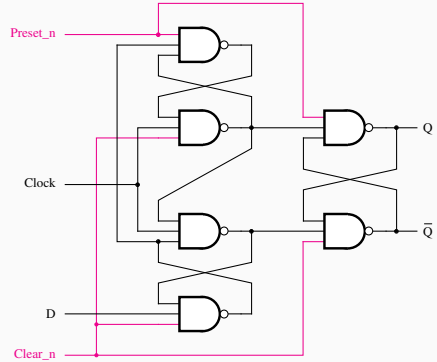
(a) Circuit



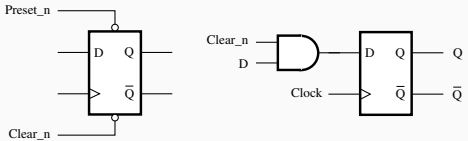
(b) Graphical symbol

Figure 5.12 Master-slave D flip-flop with *Clear* and *Preset*.

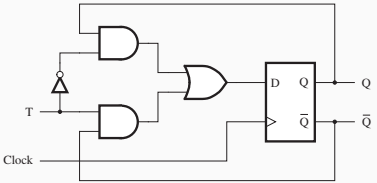
Flip-flop D Mestre/Escravo com borda positiva



(a) Circuit



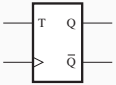
Flip-flop T



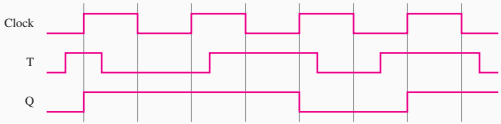
(a) Circuit

T	$Q(t+1)$
0	$Q(t)$
1	$\overline{Q}(t)$

(b) Characteristic table



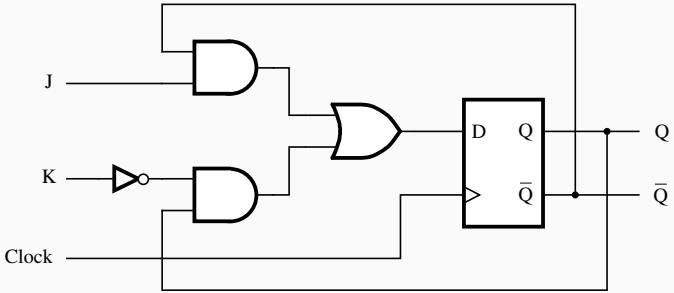
(c) Graphical symbol



(d) Timing diagram

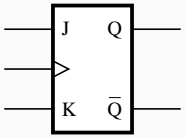
Figure 5.15 T flip-flop.

Flip-flop JK



(a) Circuit

J	K	Q$(t+1)$
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{\text{Q}}(t)$



Bibliografia

- Brown, S. & Vranesic, Z. - Fundamentals of Digital Logic with Verilog Design, 3rd Ed., Mc Graw Hill, 2009
- https://www.falstad.com/circuit/e-nandff.html

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