

# Lógica Digital (1001351)

## Circuitos Sequenciais: Registradores

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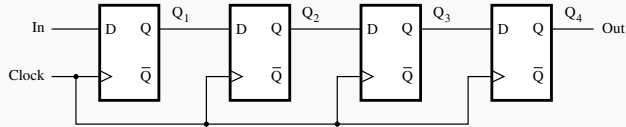
# Circuitos Sequenciais

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Nesta aula vamos aprender sobre:

- Registradores, os quais armazenam vários bits;
- Registradores de deslocamento;
- Contadores de vários tipos.

# Registrador de deslocamento



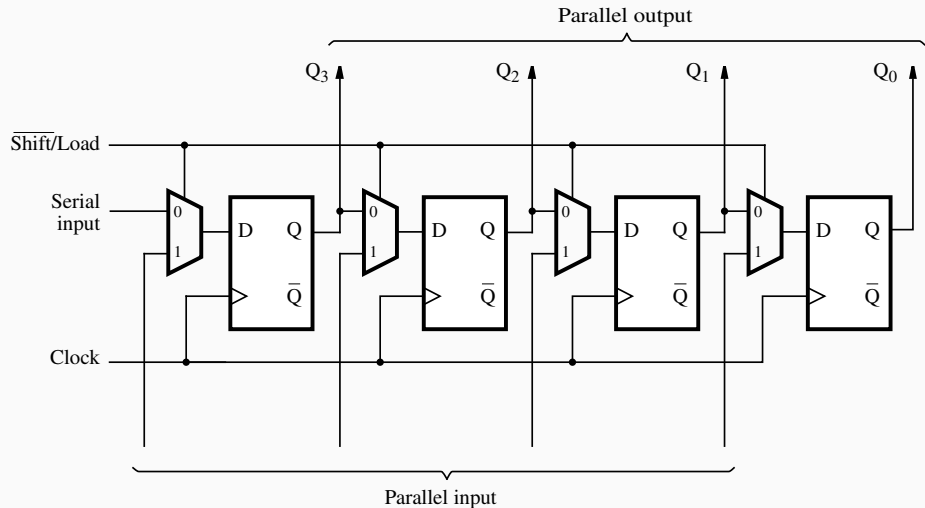
(a) Circuit

	In	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub> = Out
$t_0$	1	0	0	0	0
$t_1$	0	1	0	0	0
$t_2$	1	0	1	0	0
$t_3$	1	1	0	1	0
$t_4$	1	1	1	0	1
$t_5$	0	1	1	1	0
$t_6$	0	0	1	1	1
$t_7$	0	0	0	1	1

(b) A sample sequence

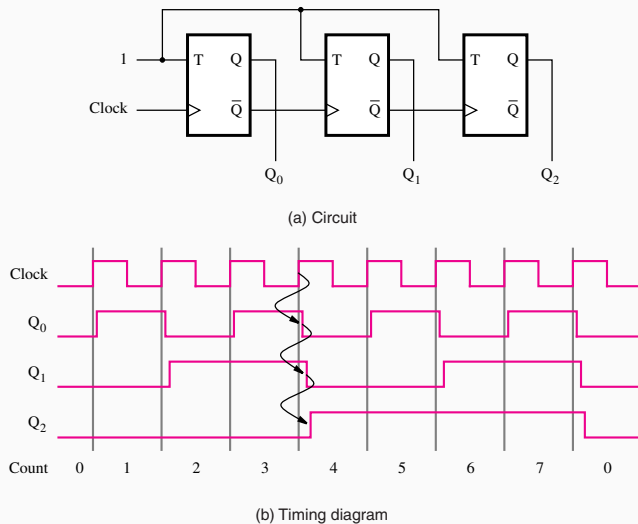
**Figure 5.17** A simple shift register.

# Registrador de deslocamento com carga paralela



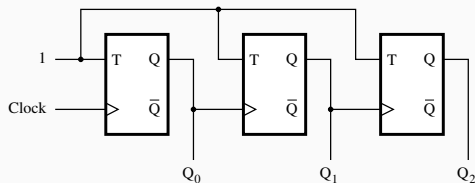
**Figure 5.18** Parallel-access shift register.

# Contador de três bits

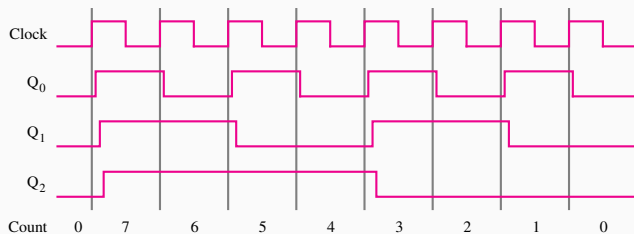


**Figure 5.19** A three-bit up-counter.

## Contador de três bits (decremento)



(a) Circuit



(b) Timing diagram

**Figure 5.20** A three-bit down-counter.

**Table 5.1** Derivation of the synchronous up-counter.

Clock cycle	$Q_2$	$Q_1$	$Q_0$
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

$$T_0 = 1$$

$$T_1 = Q_0$$

$$T_2 = Q_0 Q_1$$

$$T_3 = Q_0 Q_1 Q_2$$

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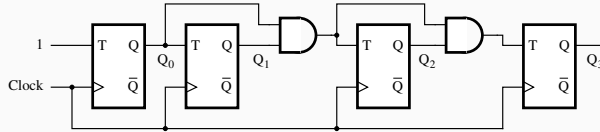
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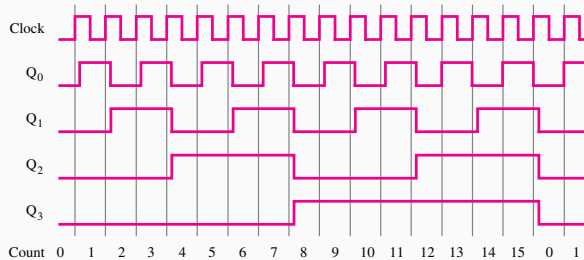
$$T_n = Q_0 Q_1 \dots Q_{n-1}$$



# Contador de 4 bits síncrono



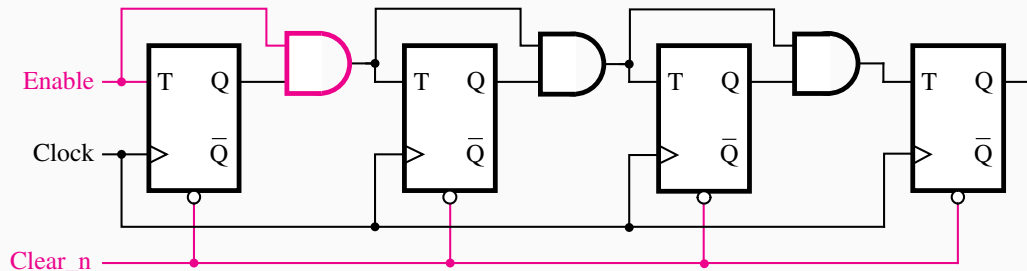
(a) Circuit



(b) Timing diagram

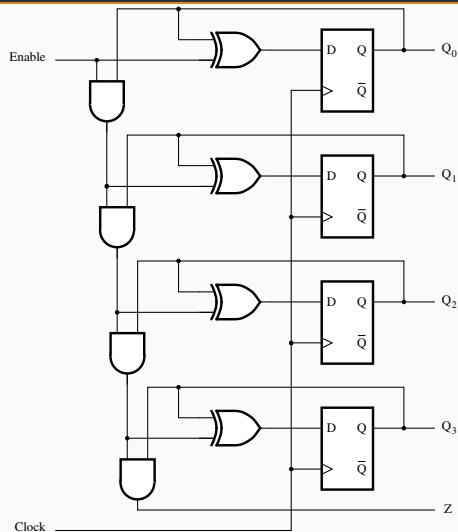
**Figure 5.21** A four-bit synchronous up-counter.

## Contador de 4 bits síncrono com *enable*



**Figure 5.22** Inclusion of Enable and Clear capability.

## Usando flip-flops do tipo D



**Figure 5.23** A four-bit counter with D flip-flops.

$$D_0 = Q_0 \oplus 1 = \bar{Q}_0$$

$$D_1 = Q_1 \oplus Q_0$$

$$D_2 = Q_2 \oplus Q_1 Q_0$$

$$D_3 = Q_3 \oplus Q_2 Q_1 Q_0$$

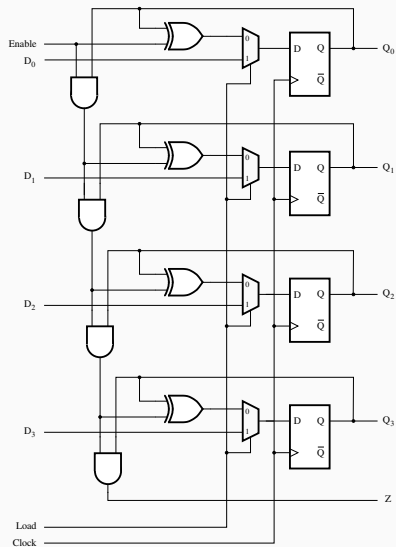
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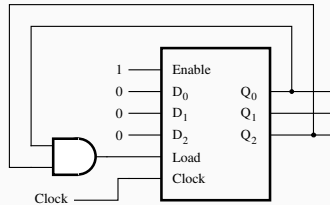
$$D_i = Q_i \oplus Q_{i-1} Q_{i-2} \dots Q_1 Q_0$$

# Contador com carga paralela

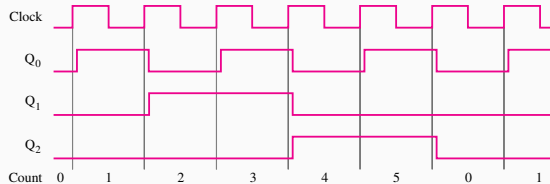


**Figure 5.24** A counter with parallel-load capability.

# Contador módulo-6 com reset síncrono



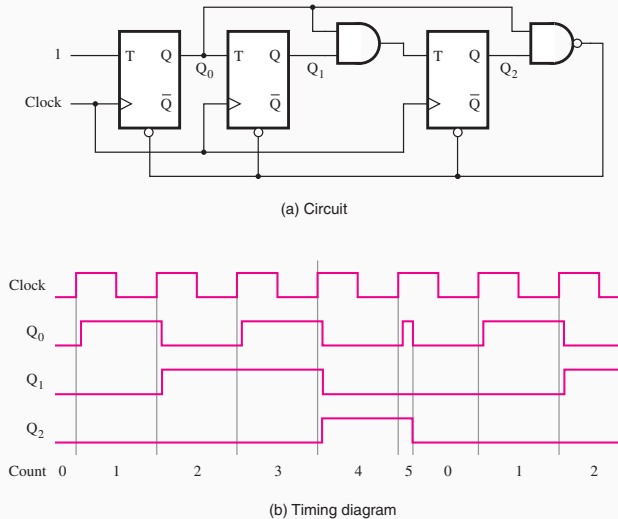
(a) Circuit



(b) Timing diagram

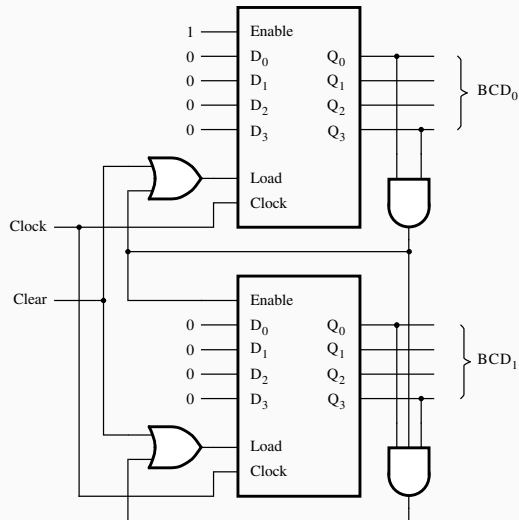
**Figure 5.25** A modulo-6 counter with synchronous reset.

## Contador módulo-6 com reset assíncrono



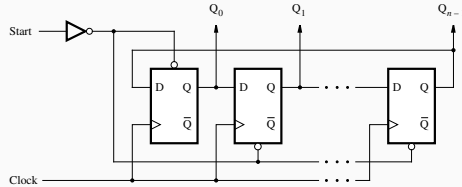
**Figure 5.26** A modulo-6 counter with asynchronous reset.

# Contador BCD de dois dígitos

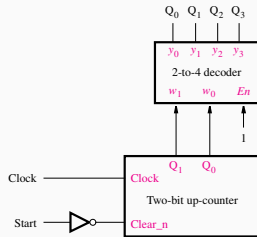


**Figure 5.27** A two-digit BCD counter.

# Contador em anel



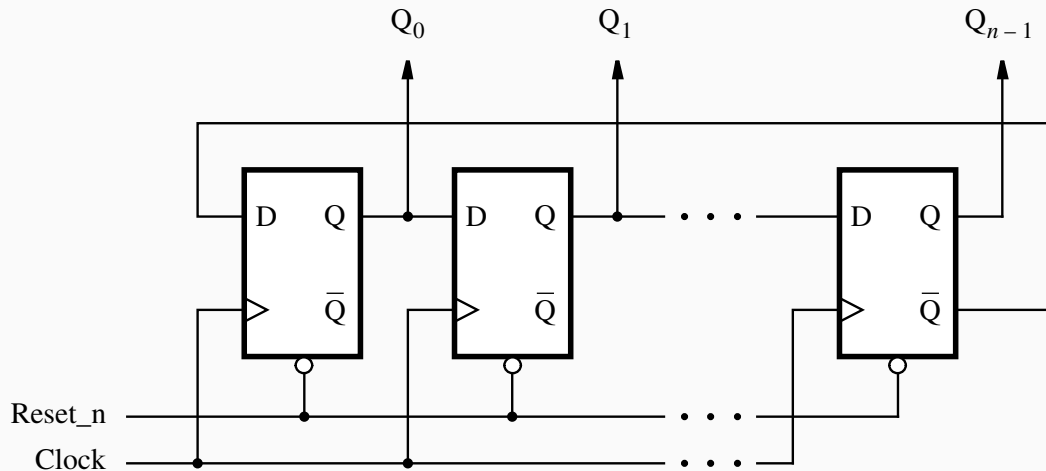
(a) An  $n$ -bit ring counter



(b) A four-bit ring counter

**Figure 5.28** Ring counter.





**Figure 5.29** Johnson counter.

- Brown, S. & Vranesic, Z. - Fundamentals of Digital Logic with Verilog Design, 3rd Ed., Mc Graw Hill, 2009
- <https://tams-www.informatik.uni-hamburg.de/applets/hades/>

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