Lógica Digital (1001351)

Circuitos Sequenciais: Máquinas de Estados Finitos

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figure6.29.v

```
1  module simple (Clock, Resetn, w, z);
2    input Clock, Resetn, w;
3    output z;
4    reg [2:1] y, Y;
5    parameter [2:1] A = 2'b00, B = 2'b01, C = 2'b10;
6    // Define the next state combinational circuit
7    always @(w, y)
8      case (y)
9        A: if (w)  Y = B;
10          else    Y = A;
11       B: if (w)  Y = C;
12          else    Y = A;
13       C: if (w)  Y = C;
14          else    Y = A;
15       default:   Y = 2'bxx;
16     endcase
17   // Define the sequential block
18   always @(negedge Resetn, posedge Clock)
19     if (Resetn == 0)  y <= A;
20     else  y <= Y;
21   // Define output
22   assign z = (y == C);
23 endmodule
```

figure6.33.v

```
1  module simple (Clock, Resetn, w, z);
2    input Clock, Resetn, w;
3    output reg z;
4    reg [2:1] y, Y;
5    parameter [2:1] A = 2'b00, B = 2'b01, C = 2'b10;
6    // Define the next state combinational circuit
7    always @(w, y)
8    begin
9      case (y)
10       A: if (w)  Y = B;
11            else  Y = A;
12       B: if (w)  Y = C;
13            else  Y = A;
14       C: if (w)  Y = C;
15            else  Y = A;
16       default:   Y = 2'bxx;
17     endcase
18     z = (y == C);  //Define output
19    end
20   // Define the sequential block
21   always @(negedge Resetn, posedge Clock)
22     if (Resetn == 0)  y <= A;
23     else  y <= Y;
24 endmodule
```

figure6.34.v

```
1  module simple (Clock, Resetn, w, z);
2    input Clock, Resetn, w;
3    output z;
4    reg [2:1] y;
5    parameter [2:1] A = 2'b00, B = 2'b01, C = 2'b10;
6    // Define the sequential block
7    always @(negedge Resetn, posedge Clock)
8      if (Resetn == 0)  y <= A;
9      else
10       case (y)
11         A: if (w)  y <= B;
12              else  y <= A;
13         B: if (w)  y <= C;
14              else  y <= A;
15         C: if (w)  y <= C;
16              else  y <= A;
17         default:  y <= 2'bxx;
18       endcase
19   // Define output
20   assign z = (y == C);
21 endmodule
```

figure6.35.v

```
1  module control (Clock, Resetn, w, R1in, R1out, R2in, R2out, R3in, R3out,Done);
2    input Clock, Resetn, w;
3    output R1in, R1out, R2in, R2out, R3in, R3out, Done;
4    reg [2:1] y, Y;
5    parameter [2:1] A = 2'b00, B = 2'b01, C = 2'b10, D = 2'b11;
6    // Define the next state combinational circuit
7    always @(w, y)
8      case (y)
9        A: if (w)  Y = B;
10            else  Y = A;
11       B:  Y = C;
12       C:  Y = D;
13       D:  Y = A;
14     endcase
15   // Define the sequential block
16   always @(negedge Resetn, posedge Clock)
17     if (Resetn == 0)  y <= A;
18     else  y <= Y;
19   // Define outputs
20   assign R3in = (y == B);  assign R3out = (y == D);
21   assign R2in = (y == C);  assign R2out = (y == B);
22   assign R1in = (y == D);  assign R1out = (y == C);
23   assign Done = (y == D);
24 endmodule
```

figure6.36.v

```
1  module mealy (Clock, Resetn, w, z);
2    input Clock, Resetn, w;
3    output reg z;
4    reg y, Y;
5    parameter A = 1'b0, B = 1'b1;
6    // Define the next state and output combinational circuits
7    always @(w, y)
8      case (y)
9        A:  if (w) begin
10           z = 0;  Y = B;
11           end
12         else begin
13           z = 0;  Y = A;
14            end
15       B:  if (w) begin
16           z = 1;  Y = B;
17           end
18         else begin
19           z = 0;  Y = A;
20         end
21     endcase
22   // Define the sequential block
23   always @(negedge Resetn, posedge Clock)
24     if (Resetn = = 0) y <= A;
25     else   y <= Y;
26 endmodule
```

Bibliografia

- Brown, S. & Vranesic, Z. - Fundamentals of Digital Logic with Verilog Design, 3rd Ed., Mc Graw Hill, 2009

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