Lógica Digital (1001351)

Máquinas de Estados Finitos: Minimização

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Definições

Dois estados S_i e S_j são ditos equivalentes se e somente se para cada sequência de entradas possível, a mesma sequência de saída será produzida independente de se partir de S_i ou S_j.

Uma partição consiste em um ou mais blocos, onde cada bloco constitui um subconjunto de estados que podem ser equivalentes, mas os estados em um dado bloco são definitivamente não equivalentes aos estados de outro bloco.

Present state	Next state		Output
	$w = 0$	$w = 1$	z
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

$P_1 = (ABCDEFG)$

Figure 6.51 State table for Example 6.6.

Present state	Next state		Output
	$w = 0$	$w = 1$	z
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

$P_1 = (ABCDEFG)$
$P_2 = (ABD)(CEFG)$

Figure 6.51 State table for Example 6.6.

Present state	Next state		Output
	$w = 0$	$w = 1$	z
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

$P_1 = (ABCDEFG)$
$P_2 = (ABD)(CEFG)$
$P_3 = (ABD)(CEG)(F)$

Figure 6.51 State table for Example 6.6.

Present state	Next state		Output
	$w = 0$	$w = 1$	z
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

$P_1 = (ABCDEFG)$
$P_2 = (ABD)(CEFG)$
$P_3 = (ABD)(CEG)(F)$
$P_4 = (AD)(B)(CEG)(F)$

Figure 6.51 State table for Example 6.6.

Present state	Next state		Output
	$w = 0$	$w = 1$	z
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

$P_1 = (ABCDEFG)$
$P_2 = (ABD)(CEFG)$
$P_3 = (ABD)(CEG)(F)$
$P_4 = (AD)(B)(CEG)(F)$
$P_5 = P_4$

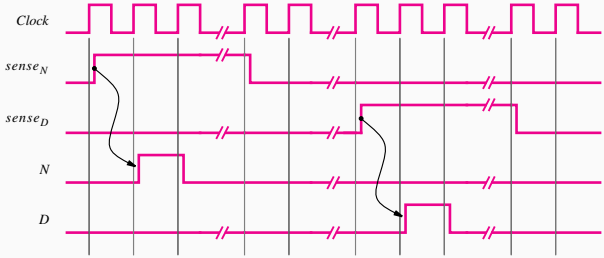
Figure 6.51 State table for Example 6.6.

Present state	Next state		Output
	$w = 0$	$w = 1$	z
A	B	C	1
B	A	F	1
C	F	C	0
F	C	A	0

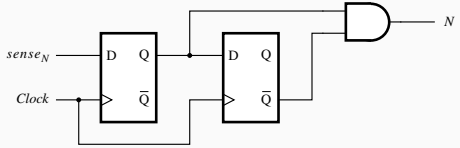
$P_1 = (ABCDEFG)$
$P_2 = (ABD)(CEFG)$
$P_3 = (ABD)(CEG)(F)$
$P_4 = (AD)(B)(CEG)(F)$
$P_5 = P_4$

Figure 6.52 Minimized state table for Example 6.6.

Vending machine



(a) Timing diagram



(b) Circuit that generates N

Figure 6.53 Signals for the vending machine.

Vending machine

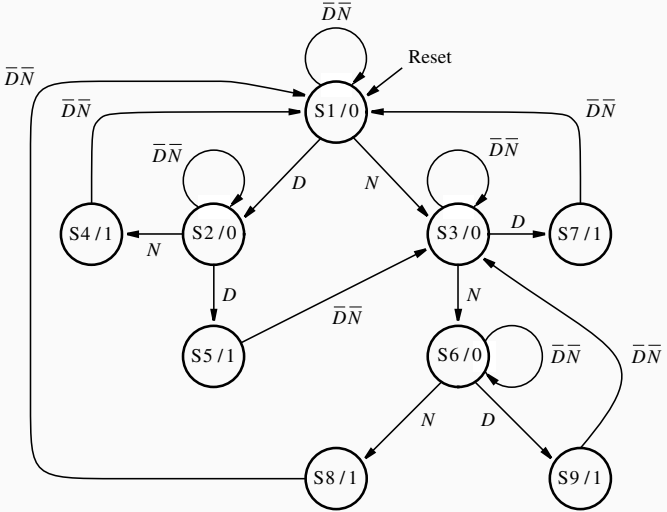


Figure 6.54 State diagram for Example 6.7.

Particionamento

Present state	Next state				Output
	DN = 00	01	10	11	z
S1	S1	S3	S2	–	0
S2	S2	S4	S5	–	0
S3	S3	S6	S7	–	0
S4	S1	–	–	–	1
S5	S3	–	–	–	1
S6	S6	S8	S9	–	0
S7	S1	–	–	–	1
S8	S1	–	–	–	1
S9	S3	–	–	–	1

$P_1 = (S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8, S_9)$
$P_2 = (S_1, S_2, S_3, S_6)(S_4, S_5, S_7, S_8, S_9)$
$P_3 = (S_1)(S_3)(S_2, S_6)(S_4, S_5, S_7, S_8, S_9)$
$P_4 = (S_1)(S_3)(S_2, S_6)(S_4, S_7, S_8)(S_5, S_9)$
$P_5 = P_4$

Figure 6.55 State table for Example 6.7.

Particionamento

Present state	Next state				Output
	$DN = 00$	01	10	11	z
S1	S1	S3	S2	—	0
S2	S2	S4	S5	—	0
S3	S3	S2	S4	—	0
S4	S1	—	—	—	1
S5	S3	—	—	—	1

$$P_1 = (S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8, S_9)$$
$$P_2 = (S_1, S_2, S_3, S_6)(S_4, S_5, S_7, S_8, S_9)$$
$$P_3 = (S_1)(S_3)(S_2, S_6)(S_4, S_5, S_7, S_8, S_9)$$
$$P_4 = (S_1)(S_3)(S_2, S_6)(S_4, S_7, S_8)(S_5, S_9)$$
$$P_5 = P_4$$

Figure 6.56 Minimized state table for Example 6.7.

Moore vs Mealy

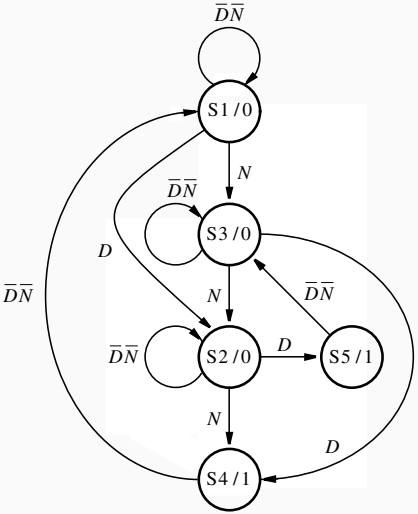


Figure 6.57 Minimized state diagram for Example 6.7.

Moore vs Mealy

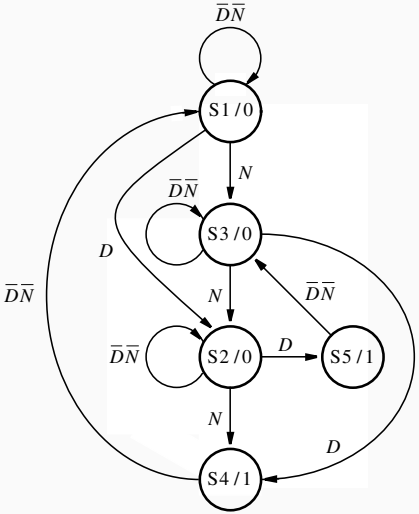


Figure 6.57 Minimized state diagram for Example 6.7.

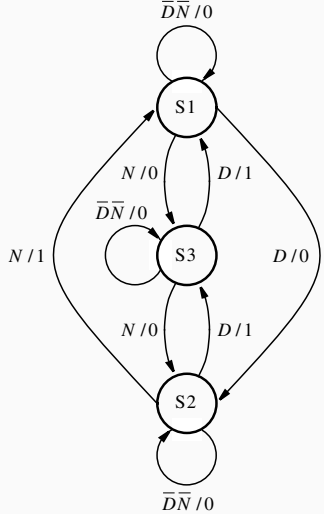


Figure 6.58 Mealy-type FSM for Example 6.7.

Particionamento de máquinas incompletas

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	B	C	0	0
B	D	—	0	—
C	F	E	0	1
D	B	G	0	0
E	F	C	0	1
F	E	D	0	1
G	F	—	0	—

$P_1 = (ABCDEFG)$
$P_2 = (ABDG)(CEF)$
$P_3 = (AB)(D)(G)(CE)(F)$
$P_4 = (A)(B)(D)(G)(CE)(F)$
$P_5 = P_4$

Particionamento de máquinas incompletas

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	B	C	0	0
B	D	—	0	—
C	F	E	0	1
D	B	G	0	0
E	F	C	0	1
F	E	D	0	1
G	F	—	0	—

$P_1 = (ABCDEFG)$
$P_2 = (ABDG)(CEF)$
$P_3 = (AB)(D)(G)(CE)(F)$
$P_4 = (A)(B)(D)(G)(CE)(F)$
$P_5 = P_4$

$P_1 = (ABCDEFG)$
$P_2 = (AD)(BCEFG)$
$P_3 = (AD)(B)(CEFG)$
$P_4 = (AD)(B)(CEG)(F)$
$P_5 = P4$

Bibliografia

- Brown, S. & Vranesic, Z. - Fundamentals of Digital Logic with Verilog Design, 3rd Ed., Mc Graw Hill, 2009

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